MOTOROLA

MC13081X

Advance Information

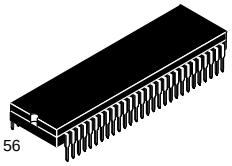
Multimode Color Monitor Horizontal, Vertical, and Video Combination Processor

MULTIMODE COLOR MONITOR PROCESSOR

SEMICONDUCTOR TECHNICAL DATA

The MC13081X includes all the signal processing functions for a scan frequency agile and multiple sync system analog RGB monitor and includes the following functions:

- Automatic Horizontal Frequency Tracking of All Commonly Used Personal Computers, Continuously Adaptable from 30 kHz to 64 kHz
- Sync–on–Green Detection
- Vertical Timebase Operates from 45 to 100 Hz
- Vertical and Horizontal Sync Polarity Detection with Outputs for Mode Switching
- Video Pre–Amplifiers Typical Rise/Fall Time of 5.0 ns at 3.0 Vpp Output Voltage Swing
- Overall Contrast Control and Independent RGB Gain Controls

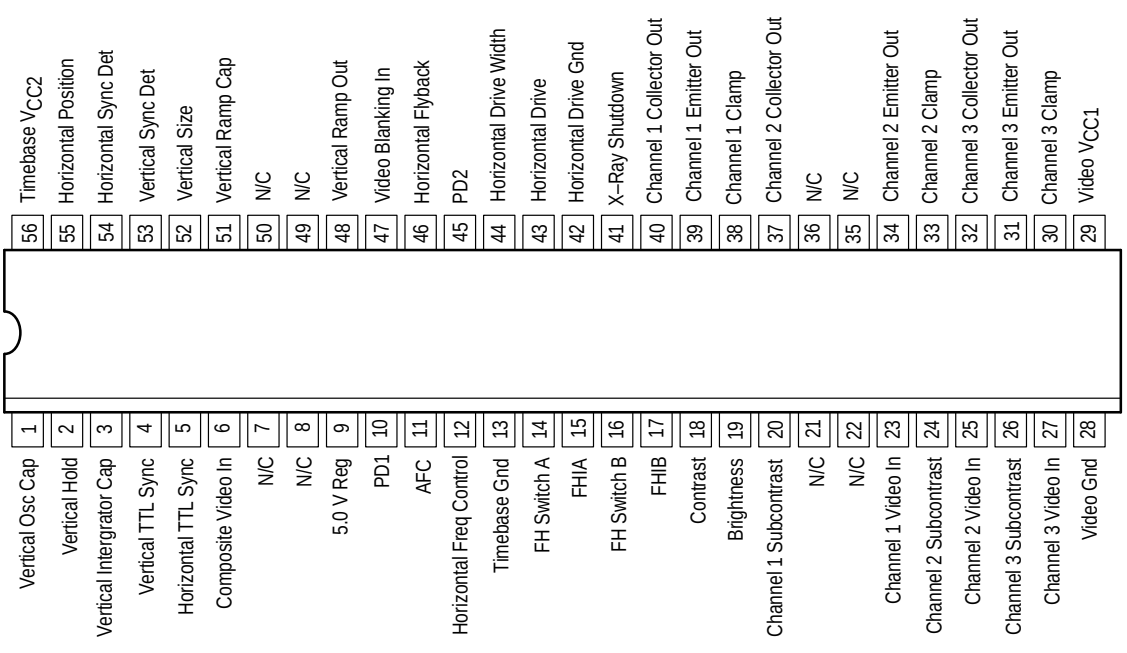


B SUFFIX
PLASTIC SDIP PACKAGE
CASE 859

ORDERING INFORMATION

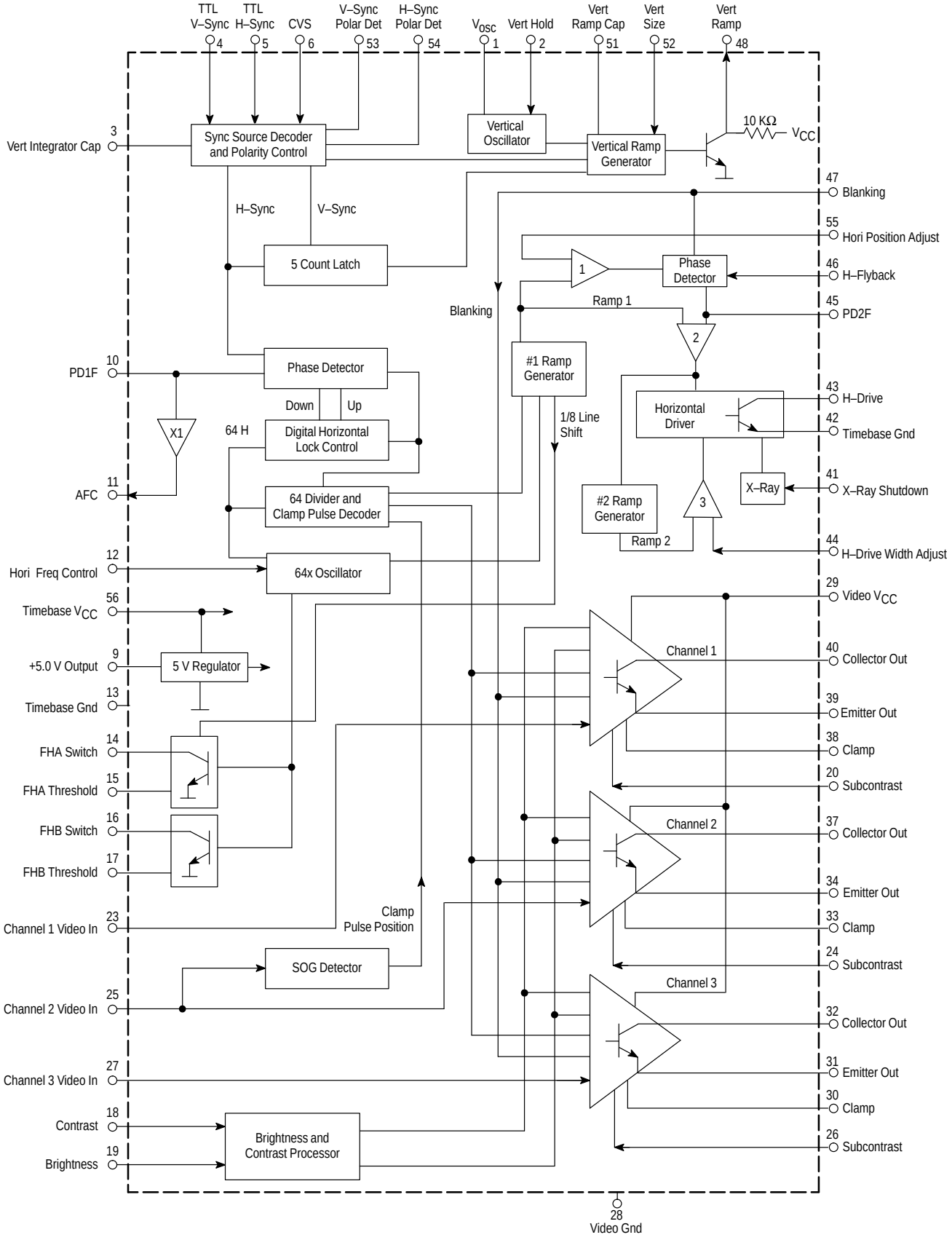
Device	Operating Temperature Range	Package
MC13081XB	T_A = 0° to +70°C	Plastic SDIP

PIN CONNECTIONS



(Top View)

Figure 1. Block Diagram



This device contains 1074 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage Video Section V_{CC1} Timebase Section V_{CC2}	 29 56	 –0.5, +10 –0.5, +10	Vdc
Brightness, Contrast, Horizontal Flyback Input, Frequency Switch when Off	19, 18, 46, 14, 16	0 to V_{CC}	Vdc
X–Ray Shutdown	41	–0.5, +0.9	Vdc
Subcontrast RGB Controls	20, 24, 26	0 to +2.0	Vdc
Horizontal Drive Width, Horizontal Position	44, 55	0 to +5.0	Vdc
Voltage on Horizontal Drive when Off, Vertical TTL Sync Input, Horizontal TTL Sync Input, Composite Video Sync Input, Video Amplifier Output Collectors	43, 4, 5, 6, 32, 37, 40	–0.5 to V_{CC} + 0.5	Vdc
Current into Horizontal Drive when On	43	100	mA
Current into Frequency Switch when On	14, 16	30	mA
Video Amplifier Inputs	23, 25, 27	–0.5, + 5.0	Vdc
Video Amplifier Output Current (Total for the Three Channels)	40, 39, 37, 34, 32, 31	120	mA
Storage Temperature	–	–65 to +150	°C
Junction Temperature	–	+150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Min	Typ	Max	Unit
Power Supply Voltage Video Section V_{CC1} Timebase Section V_{CC2}	 29 56	 7.6 7.6	 8.0 8.0	 8.4 8.4	Vdc
Power Supply Voltage Difference, $V_{CC2} – V_{CC1}$	–	–0.3	0	0.8	Vdc
Internal 5.0 V Regulator Output Current	9	–20	–	0	mA
Contrast Control	18	0	–	5.0	Vdc
Brightness Control	19	0	–	5.0	Vdc
Subcontrast Control	20, 24, 26	0	–	2.0	Vdc
Horizontal Drive Width Adjust	44	0	–	5.0	Vdc
Horizontal Position Adjust	55	1.0	–	4.0	Vdc
Horizontal Flyback Signal Amplitude	46	0.7	5.0	8.0	V
Horizontal Flyback Signal DC Input Voltage Level	46	–0.2	0	–	Vdc
Voltage on Horizontal Drive Collector when “Off”	43	0	–	V_{CC}	V
Current into Horizontal Drive Collector when “On”	43	0	–	40	mA
Voltage on Horizontal Drive Emitter W.R.T. Circuit Ground	42	–0.3	0	2.0	Vdc
Blanking Input Signal Amplitude	47	1.5	–	4.0	V
Voltage on FH Switches when “Off”	14, 16	0	–	8.0	Vdc
Current into each FH Switch when “On”	14, 16	0	–	20	mA
X–Ray Shutdown	41	0	–	0.7	Vdc
Composite Video Sync Input	6	1.0	–	2.0	Vpp
Vertical Sync Frequency	–	45	–	100	Hz
Horizontal Sync Frequency	–	30	–	64	kHz
Vertical Sync Pulse Width	–	–	70	–	µs
Horizontal Sync Pulse Width	–	–	1.0	–	µs

RECOMMENDED OPERATING CONDITIONS (continued)

Characteristic	Pin	Min	Typ	Max	Unit
Video Signal Amplitude (with 75 Ω Termination)	23, 25, 27	0.5	0.7	1.2	Vpp
Voltage on Video Amplifier Collector	32, 37, 40	4.5	–	V_{CC}	Vdc
Current Through Video Collector–Emitter	40, 39, 37 34, 32, 31	0	–	40	mA
Vertical Hold Set Resistance, R9 + VR2 (Figure 2)	2	–	10	–	kΩ
Vertical Size Set Resistance, R10 + VR3 (Figure 2)	52	–	220	–	kΩ
Vertical Linearity Set Resistance, R12 + VR4 (Figure 2)	51	–	1000	–	kΩ
Operating Ambient Temperature	–	0	25	70	°C
FH Switches Set Resistance	15, 17	See Application Section 5			–
Vertical TTL Sync Input	4	TTL Voltage Level			Vdc
Horizontal TTL Sync Input	5	TTL Voltage Level			Vdc

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
POWER SUPPLIES						
Supply Current Total Consumption	–	29, 56	70	85	110	mA
5.0 V Regulator		9				
Output Voltage	Load Current (I_B) = 0 mA		4.75	5.0	5.25	Vdc
Line Regulation	7.6 V < V_{CC} < 8.4 V, I_B = 0 mA		–	25	–	mV
Load Regulation	–10 mA < I_B < 0 mA		–	100	–	mV
Temperature Coefficient			–	–0.3	–	mV/°C
Thermal Resistance, Junction–to–Ambient	–	–	–	59	–	°C/W
HORIZONTAL PROCESSING						
Horizontal Oscillator Frequency Range	–	43	30	–	64	kHz
Horizontal Oscillator Free Running Frequency @ I12 = 240 μA	Sink 240 μA from Pin 12 with Resistor R5 Opened	43	29	31	33	kHz
Horizontal Sync Detector Output/+V_E Sync	–	54	–	0	–	Vdc
Horizontal Sync Detector Output/–V_E Sync	–	54	–	3.6	–	Vdc
Horizontal Sync Input	–	5				
Input Impedance			–	22	0	kΩ
Input Level – Low			0	–	0.8	Vdc
Input Level – High			2.4	–	5.0	Vdc
Composite Video Sync Input	–	6				
Input Impedance			–	1.0	–	kΩ
Internal Bias Level			–	1.55	–	Vdc
Minimum Input Amplitude			0.1	–	–	Vpp
Short Term Horizontal Pull–In Range	Time < 5.0 ms	–	–	±5.0	–	%FH
Long Term Horizontal Pull–In Range	Time > 500 ms	–	30	–	64	kHz
Horizontal Frequency Control (Current Transfer Constant)	Current Flowing Out of Pin 12	12	115	122	129	Hz/μA
Horizontal Free Running Frequency Change versus Temperature	Pin 11 is Opened	–	–	300	–	ppm/°C
FH Switch Threshold Pins	–	15, 17				
Output Current			–	I12/2	–	μA
Threshold			–	5.0	–	V
Hysteresis			0	–	200	mV
FH Switch Voltage when “On”	I = 10 mA	14, 16	–	–	200	mVdc

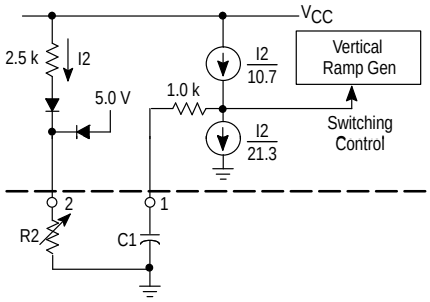
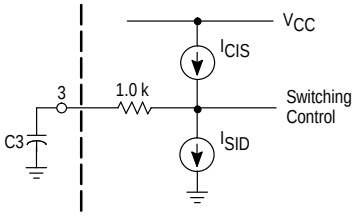
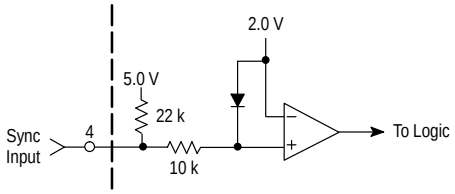
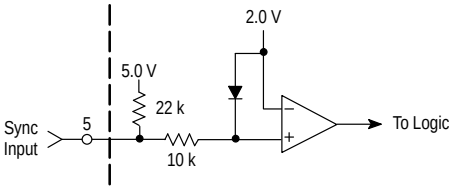
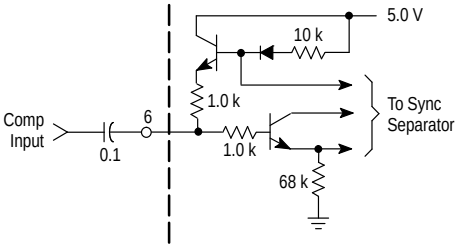
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
HORIZONTAL DRIVE						
Horizontal Position Adjust	0 < V55 < 5.0 V,	55				
Range	FH = 30 k – 56 kHz		–	10	–	%
Input Impedance	See Application Section 7		–	31	–	kΩ
Horizontal Drive Width Adjust	FH = 35 kHz, 0 < V44 < 5.0 V	44				
Range			2:1	–	1:2	%
Input Impedance			–	30	–	kΩ
Horizontal Flyback	See Application Section 4	46				
Threshold	Input Signal Should Not Fall		–	0.7	–	V
Input Amplitude	Below –0.2 V		0	–	8.0	V
Input Impedance			–	10	–	kΩ
Horizontal Drive		43				
Output Low	I_{sink} = 40 mA		0	–	0.3	Vdc
Output High	V43 = V_{CC}		–	–	100	μA
Time Delay from Flyback to Video Output Blanking	See Application Section 7	–	–	250	–	ns
Time Delay from Blanking to Video Output Blanking	See Application Section 7	–	–	400	–	ns
X–Ray Shutdown Activate Voltage	See Application Section 11	41	0.4	0.58	0.7	Vdc
Temperature Coefficient of X–Ray Threshold Voltage	–	41	–	–2.3	–	mV/°C
Horizontal Jitter	30 kHz < FH < 56 kHz	43	–	3.0	–	ns
VERTICAL PROCESSING						
Vertical Ramp Frequency	–	48	45	–	100	Hz
Vertical Ramp	FV = 50 Hz,	48				
Amplitude	R12 + VR4 = 820 kΩ		–	3.0	–	Vpp
Minimum Peak	R10 + VR3 =120 kΩ,		–	1.9	–	V
Maximum Peak	C6 = C7 = 1.0 μF		–	3.4	–	V
Output Current			–	2.0	–	mA
Non–Linearity			–	0.45	1.0	%
Vertical Ramp Free Running Temperature Drift	FV = 50 Hz	48	–	0.01	–	Hz/°C
Vertical Ramp Free Running Drift with V_{CC}	FV = 50 Hz	48	–	0.5	–	Hz/V
Vertical Ramp Discharge Rate (Retrace)	FV = 50 Hz	48	–	9.5	–	V/ms
Vertical Sync Detector Output/+V_E Sync		53	–	0	–	Vdc
Vertical Sync Detector Output/–V_E Sync		53	–	3.6	–	Vdc
Vertical Sync Input	–	4				
Input Impedance			–	22	–	kΩ
Input Level – Low			0	–	0.8	Vdc
Input Level – High			2.4	–	5.0	Vdc
VIDEO AMPLIFIERS						
Input Impedance	–	23, 25,27	100	–	–	kΩ
Internal DC Bias Voltage			–	2.4	–	Vdc
Output Signal Amplitude	V_{in} = 0.7 Vpp, V18 = 5.0 V	39, 34, 31	–	3.6	–	Vpp
Voltage Gain	V20 = V24 = V26 = 0 V		–	5.1	–	V/V
Contrast Control	V18 = 0 to 5.0 V; V20, 24, 26 = 0 V	18	–	20	–	dB
Subcontrast Control	V20, 24, 26 = 2.0 to 0 V; V18 = 5.0 V	20, 24, 26	1:2.5	–	–	–
Brightness Control	V19 = 0 to 5.0 V, Measure Pin 39, 34, 31 DC Level	19	–	±0.5	–	Vdc

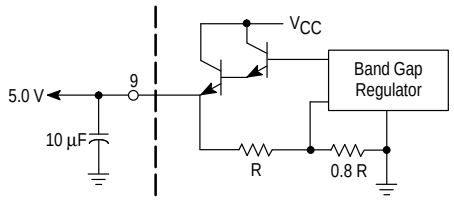
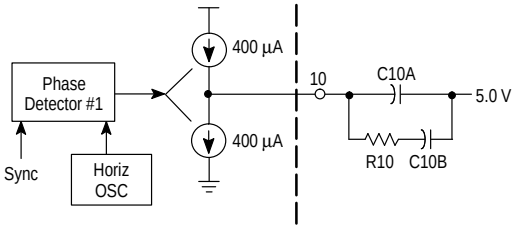
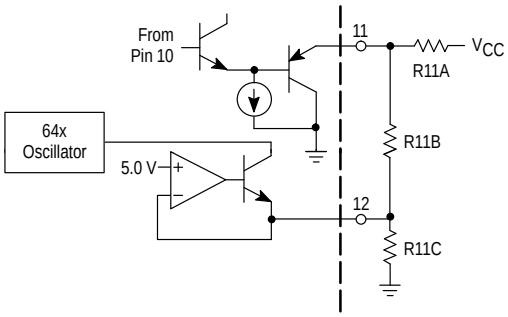
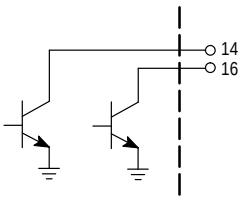
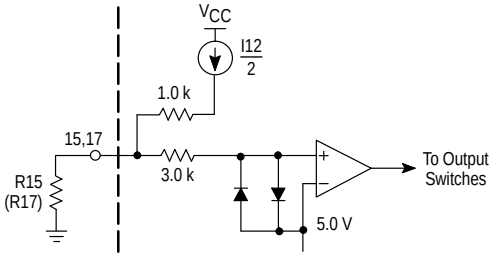
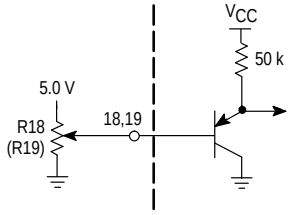
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
VIDEO AMPLIFIERS						
Emitter DC Level		39, 34, 31				Vdc
Minimum Brightness	V19 = 0 V		–	1.0	–	
Nominal Brightness	V19 = 2.5 V		1.25	1.5	1.75	
Maximum Brightness	V19 = 5.0 V		–	2.0	–	
Crosstalk, Amplifier to Amplifier	Frequency = 10 MHz	39, 34, 31	–	34	–	dB
Output Rise Time	V_{in} = 0.7 Vpp; V_{out} = 3.0 Vpp	39, 34, 31	–	5.0	–	ns
Output Fall Time			–	5.0	–	

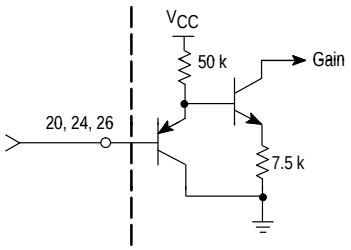
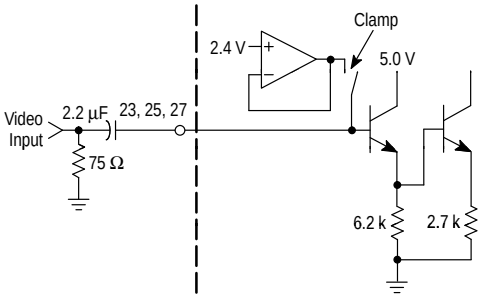
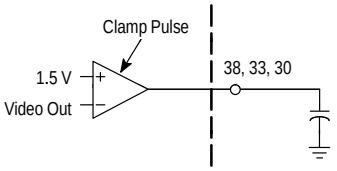
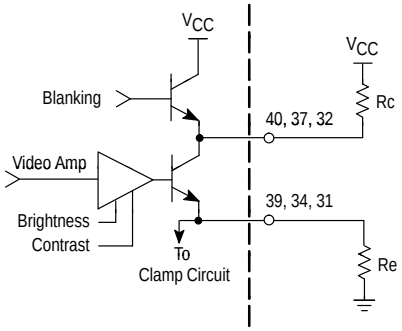
PIN FUNCTION DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
1	Vertical Oscillator Capacitor		This capacitor should be 100 nF film type to give good temperature stability.
2	Vertical Hold Control		The potentiometer at Pin 2 adjusts the free running frequency of the oscillator. It should normally be set for about 55 Hz with no vertical signal input such that it will lock to 60 Hz.
3	Vertical Integrator Capacitor		The capacitor on this pin integrates the sync pulses with a long time constant. C3 is typically 0.01 µF.
4	Vertical TTL Sync		Vertical TTL Sync input. The input threshold voltage at this pin is 2.0 V.
5	Horizontal TTL Sync		Composite or Horizontal TTL Sync input. The input threshold voltage at this pin is 2.0 V.
6	Composite Video Input		This pin requires a coupling of min 100 nF. The composite sync input should consist of $-V_E$ sync signal only with amplitude > 500 mVpp. The source impedance of the sync signal should be <1.0 kΩ. Sync information at Pin 5 will override this pin, but signals at Pin 4 will not. Minimum pulse width is 2.0 µs.
7, 8	N/C		These two pins are internally connected to each other, and nothing else.

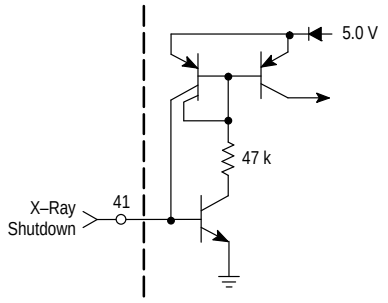
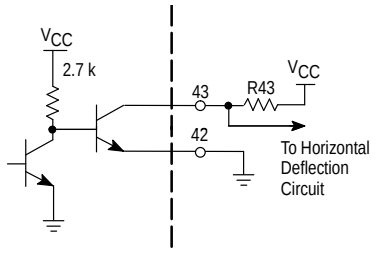
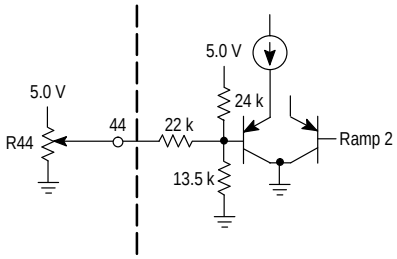
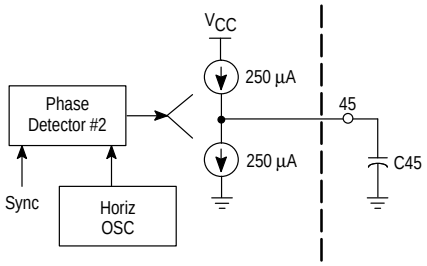
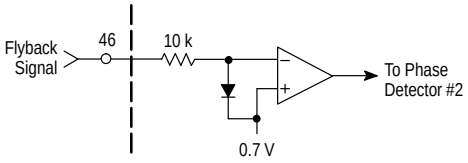
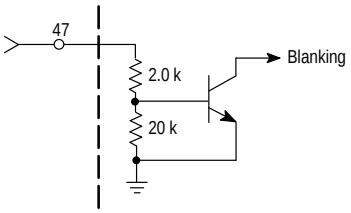
PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
9	5.0 V Regulator Output		5.0 V (±5%) regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. Up to 20 mA can be supplied to external circuitry. It can source but not sink current. Output impedance is ≈ 10 Ω. This 5.0 V regulator is recommended for use as a reference only.
10	Phase Detector 1 Filter		External components at this pin will determine the PLL gain and phase characteristics. The capacitors should be non–polarized. The voltage at this pin nominally ranges from 1.5 V to 5.0 V with corresponding horizontal frequency from 25 kHz to 68 kHz.
11	Automatic Frequency Control		Pin 11 is a buffered equivalent of Pin 10, and ranges from a minimum of 1.5 V at horizontal high frequency to near 5.0 V at low frequency. Pin 11 can sink a maximum of 1.0 mA, but cannot source current.
12	Horizontal Frequency Range		The current out of Pin 12 determines the horizontal frequency by a current transfer constant of ≈ 122 Hz/µA. Pin 12 is internally maintained at 5.0 V.
13	Timebase Ground		Ground for the timebase section. Connect to a clean, low impedance ground.
14, 16	FH Switch A, B		Pin 14 (Switch A), and Pin 16 (Switch B) are open collector NPN switches to ground. Each switch is “on” when the horizontal frequency is higher than the set points set by resistors at Pins 15 and 17, respectively. Maximum voltage is 8.0 V, and maximum sink current is 20 mA.
15, 17	FH Switch A, B Threshold Setting		Pin 15 and Pin 17 are current mirror at 1/2 of Pin 12 current. External resistors at these pins set the horizontal frequency at which Pins 14 and 16 will switch, respectively. The threshold voltage is 5.0 V.
18	Contrast Control		The input control range is from 0 to 5.0 V. An increase of voltage increases contrast.
19	Brightness Control		The input control range is from 0 to 5.0 V. An increase of voltage increases brightness.

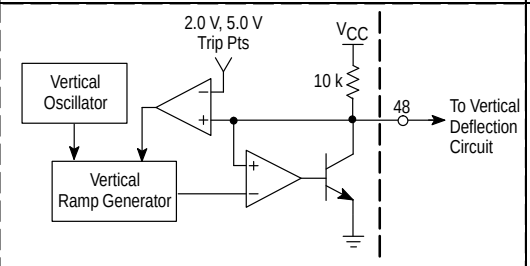
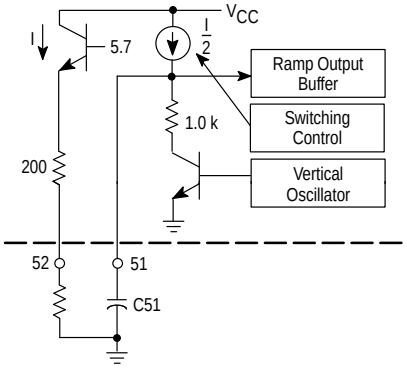
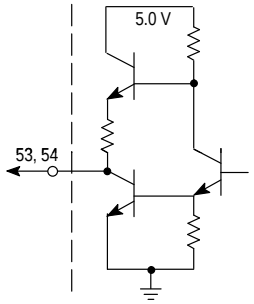
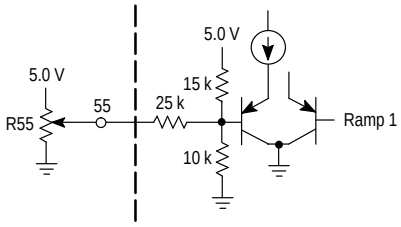
PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
20 24 26	Subcontrast Control Channel 1 Channel 2 Channel 3		Subcontrast controls the gain of each video channel. 0 V for maximum gain, and 2.0 V for minimum gain.
21, 22	N/C		These two pins are internally connected to each other, and nothing else.
23 25 27	Video Inputs Channel 1 Channel 2 Channel 3		The input coupling capacitor is used for input clamp storage. The maximum source impedance is 100 Ω. Polarity of the input video signal is positive. Amplitude should be nominally 0.7 Vpp.
28	Video Ground		Ground for the video section (video amplifiers, contrast and brightness controls, subcontrast, and video reference voltage). Noise from the timebase section, and other digital circuits, should not be allowed to produce ground bounce at this pin.
29	Video V_{CC1}		Connected to a 8.0, V ±5%, dc supply. Decoupling is required at this pin.
38 33 30	Video Clamp Channel 1 Channel 2 Channel 3		Normally a 100 nF capacitor is connected to each of these pins.
39 34 31 40 37 32	Video Emitter Output Channel 1 Channel 2 Channel 3 Video Collector Output Channel 1 Channel 2 Channel 3		Pins 39, 34, and 31 are the emitter outputs of the three video amplifier, and have an internal 33 Ω resistor. The emitter dc voltage is controlled by the brightness control. The current through each collector and emitter should not exceed 40 mA.
35, 36	N/C		These two pins are internally connected to each other, and nothing else.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
41	X–Ray Shutdown		If the voltage at this pin is > 0.58 V, the horizontal driver device (Pins 42 and 43) will be “on” until power is removed, or the voltage on this pin is taken below 0.4 V.
42	Horizontal Drive Ground		This emitter pin must be connected externally to a low impedance ground. Pin 43 is an open collector pin and normally is pulled up by a resistor to V_{CC}. Maximum current through Pins 42 and 43 must be less than 40 mA.
43	Horizontal Drive		
44	Horizontal Drive Width		Varying the voltage at this pin will change the horizontal drive duty cycle. As the voltage of this pin is increased, the “on” time at Pin 43 is decreased. Input impedance is ≈ 30 kΩ.
45	Secondary Phase Detector Filter		Typically a 10 to 100 nF decoupling capacitor is connected to this pin.
46	Horizontal Flyback		The flyback signal should be a $+V_E$ pulse of peak voltage 8.0 V. The internal switching voltage is 0.7 V and it controls the secondary PLL Input impedance is ≈ 10 kΩ
47	Video Blanking Input		The video blanking signal should be positive pulse in the range of 1.5 to 4.0 V.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
48	Vertical Ramp Output		This ramp signal drives the external vertical output devices. Voltage ramps from 2.0 V to less than 5.0 V, depending on frequency and components at Pins 51 and 52. Loading on this pin must be > 30 kΩ to avoid distorting or clipping the ramp.
49, 50	N/C		These two pins are internally connected to each other, and nothing else.
51	Vertical Ramp Capacitor		The slope of the output ramp is determined by the components at Pins 51 and 52. The resistor at Pin 52 sets the charging current of the capacitor, and therfore the vertical height of the picture. The linearity of the ramp can be modified by external feedback.
52	Vertical Size Control		
53	Vertical Sync Polarity Detector		The output goes low when the vertical sync input polarity is positive. It goes high when the vertical sync input polarity is negative.
54	Horizontal Sync Polarity Detector		The output goes low when the horizontal sync input polarity is positive. It goes high when the horizontal sync input polarity is negative.
55	Horizontal Position Control		Varying the voltage at this pin will change the horizontal position of the picture. Input impedance is ≈ 31 kΩ.
56	Timebase V_{CC2}		Connected to a 8.0 V, ±5%, dc supply. Decoupling is required at this pin.

APPLICATION INFORMATION

The MC13081X is an integrated multisync color monitor processor. It combines horizontal/vertical deflection processing circuitry and video pre–amplifiers into a single device.

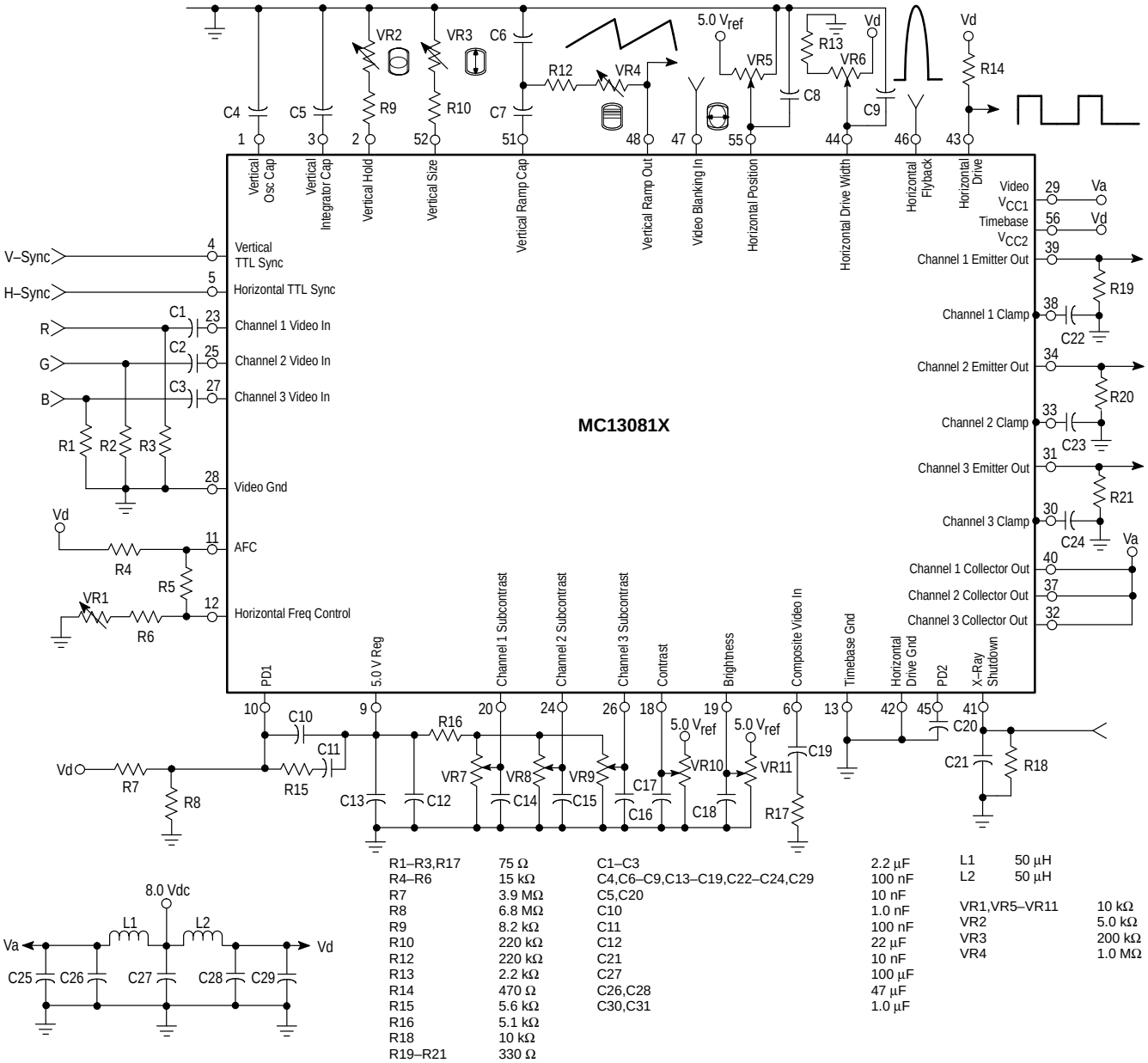
The overall timebase section consists of two parts: horizontal and vertical. The horizontal timebase can be operated from 30 kHz to 64 kHz, and can be driven from TTL separate sync, composite sync, or a composite video signal. There are two PLLs which ensure proper timing throughout the whole system. The first PLL provides line locking of the horizontal sync signal with the built–in oscillator, while the second one maintains fixed timing with the horizontal flyback signal such that a stable display can be achieved.

The vertical timebase section operates from 45 Hz to 100 Hz, and can receive various sync signals as the horizontal one does. This section consists of an oscillator and a ramp generator. Adjustments include linearity, ramp amplitude, and minimum free running frequency in the absence of sync signal.

The video section has three 70 MHz bandwidth pre–amplifiers. The outputs of these amplifiers are uncommitted collector/emitter facilitating cascode configuration with subsequent stages. Controls include brightness and contrast. In addition, the voltage gain of each amplifier can be adjusted individually which provides flexibility in adjusting color correctness. Blanking and clamping signals are provided to the amplifiers internally from the timebase section. Additionally, a blanking signal can also be supplied externally.

Separate power supply and ground pins are provided to the timebase and video section in order to minimize the cross interference between these two sections.

Figure 2. Application Circuit



R1–R3,R17	75 Ω	C1–C3	2.2 µF	L1	50 µH
R4–R6	15 kΩ	C4,C6–C9,C13–C19,C22–C24,C29	100 nF	L2	50 µH
R7	3.9 MΩ	C5,C20	10 nF		
R8	6.8 MΩ	C10	1.0 nF	VR1,VR5–VR11	10 kΩ
R9	8.2 kΩ	C11	100 nF	VR2	5.0 kΩ
R10	220 kΩ	C12	22 µF	VR3	200 kΩ
R12	220 kΩ	C21	10 nF	VR4	1.0 MΩ
R13	2.2 kΩ	C27	100 µF		
R14	470 Ω	C26,C28	47 µF		
R15	5.6 kΩ	C30,C31	1.0 µF		
R16	5.1 kΩ				
R18	10 kΩ				
R19–R21	330 Ω				

The following describes a step–by–step procedure in using the MC13801 for a typical multisync color monitor chassis; component notations refer to Figure 2.

1. Horizontal Frequency Range Resistor Network (Pins 11, 12)

F_{Hm} = Minimum Horizontal Frequency
F_{Hx} = Maximum Horizontal Frequency
Oscillator Transfer Constant = 122 Hz/μA

$$R5 = \frac{6.35 \times 10^8}{F_{Hx} - F_{Hm}}$$

$$R6 = \frac{5}{\frac{F_{Hx}}{122 \times 10^6} - \frac{3.5}{R5}}$$

$$R4 \leq \frac{V_{CC} - 6.0}{1.5} \times R5 \text{ and } \frac{V_{CC} - 1.5}{R4} < 1.0 \text{ mA}$$

For most applications, R4 = R5 provides the required results.

NOTE: In order to compensate device/component tolerance, a potentiometer is recommended in series with R6, as VR1.

2. Horizontal Frequency Range Phase Detector Filter Network (Pin 10)

Typical values are:
C10 = 1.0 nF
C11 = 100 nF
R15 = 5.6 k
C11 ≥ 100 x C10

NOTE: C10 and C11 should have less than 1.0 μA leakage.

3. Horizontal Free Running Frequency

The voltage at Pin 10 will be buffered to Pin 11, and hence control the internal oscillator. In the absence of horizontal sync signal, the free running horizontal frequency will vary between preset minimum and maximum horizontal frequency values.

If an undetermined free running frequency value is not desired, a large impedance resistor can be used to pull Pin 10 to V_{CC} or Gnd, and the free running frequency will be equal to F_{Hm} or F_{Hx}, respectively.

The free running frequency can also be set to any value within the horizontal frequency range by using a voltage divider, as R7 and R8 indicate.

$$V11 = V_D \times \frac{R7}{R7 + R8}$$

$$I12 = \frac{V11}{R6 + VR1} - \frac{V11 - 5}{5}$$

$$\text{Free Running Frequency} = I12\ \mu A \times \frac{122\ Hz}{\mu A}$$

The above formula provides the ratio of R7 and R8. The values chosen should be similar to those shown in Figure 2.

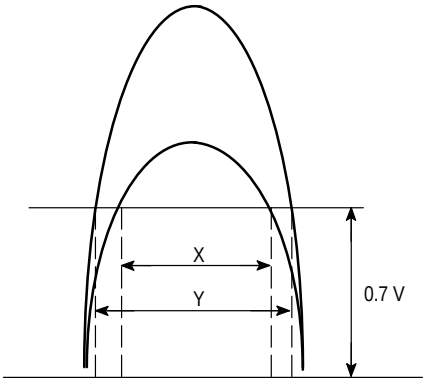
4. Horizontal Flyback Input (Pin 46)

The horizontal flyback signal not only provides proper timing reference for the horizontal drive output, but also supplies the necessary blanking for the video outputs.

There are two precautions for the flyback input. First, the signal should have a zero volt reference, and second, the peak value should be as near to V_{CC} as possible.

The threshold voltage for Pin 46 is 0.7 V. The blanking period depends on the amplitude, as shown in Figure 3 (X and Y, respectively). A larger amplitude provides better consistency and control of the blanking period.

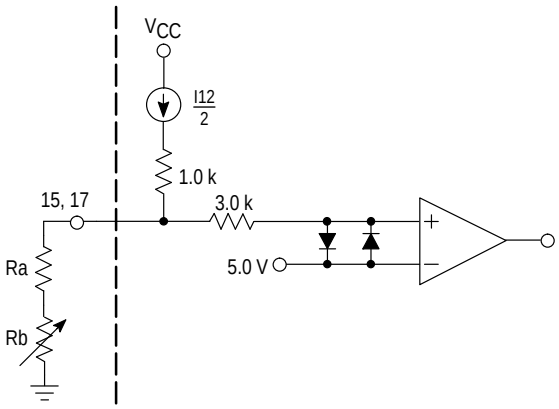
Figure 3. Voltage for Flyback



5. Frequency Switch (Pin 14 to 17)

There are two frequency switches available for screen size compensation for different timing standards. Each switch will turn on at the switch frequency set with its external resistor. See Figure 4.

Figure 4. FH Switches



The switch frequency is calculated as follow:

SF = Switch Frequency $\quad SF = \frac{5 \times 2 \times 122 \times 10^6}{Ra + Rb}$

In considering the ratio of Ra to Rb, the following parameters, and their tolerances, need to be clarified:

1. I_{osc} ±10%
2. 5.0 V_{ref} ±5%
3. V_{hys} ±5%
4. Ra, Rb ±?%

Internally, the lock–in horizontal frequency will build up a current reference, and half of this current reference is used for setting up a voltage and then compared with the internal 5.0 V_{ref}. Looking at the four parameters above, the first three are IC related, while the last item depends on the external component tolerance.

By adding up the first three items, the value of Ra and Rb should be chosen to compensate for about 20% of system tolerance.

Therefore, if Ra is chosen to be 70% of the calculated value (Ra + Rb), Rb should be 60% of (Ra + Rb). That

means, the overall adjustment is about 70% to 130%, which provides additional ±10% margin.

During normal operation, the frequency switch will switch "off" when the pin voltage falls 60 mV below the 5.0 V reference voltage (≈ 4.94 V), and will switch "on" when the pin voltage rises to 40 mV above the 5.0 V reference (≈ 5.04 V).

An Example: Require Trip Point @ 35 kHz

$$I12 = \frac{35 \text{ x } 10^3}{122} \ \mu A$$

$$\text{Trip Point Reference Current} = \frac{I12}{2}$$

$$= \frac{35 \text{ k}}{122 \text{ x } 2} \ \mu A$$

$$Ra + Rb = \frac{5.0 \text{ V}}{\frac{35 \text{ k}}{122 \text{ x } 2} \ \mu A}$$

$$= 34857 \ \Omega$$

$$\text{Hysteresis @ 35 kHz} = \frac{5.04 - 4.94 \text{ V}}{34857 \ \Omega} \text{ x } \frac{122 \text{ Hz}}{\mu A}$$

$$\approx 350 \text{ Hz}$$

From above, Ra + Rb = 34857 Ω

Select Ra = 24 k, and Rb = 20 k Trim Pot

The Temperature Coefficient of the potentiometer can also be considered. If the value of the potentiometer and Ra vary by 1% (for example) over temperature, the error would be:

$$5 \text{ x } \left\{ \frac{1}{34857 \text{ x } 0.99} - \frac{1}{34857 \text{ x } 1.01} \right\} \text{ x } \frac{122 \text{ Hz}}{\mu A}$$

$$\approx 350 \text{ Hz}$$

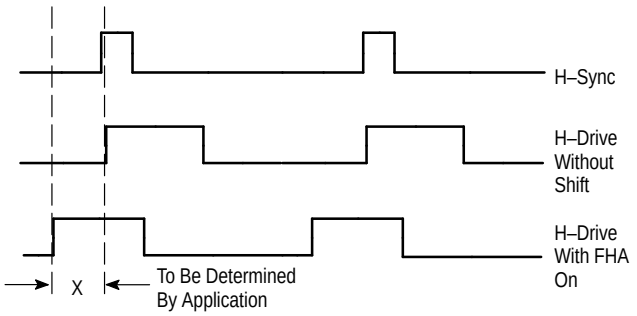
6. Horizontal Position Compensation for Selected Scan Frequency in Using FHA Switch

Refering to Figure1 (block diagram), there is an output from the FHA switch to the horizontal drive output. When the FHA switch is switched on, at a specified horizontal frequency, there is a 1/8th horizontal line shift of H–Ramp1. Referring to Figures 5 and 9, a shift of H–Ramp1 will result in a shift of the H–Drive output timing with respect to flyback input.

The exact H–Drive output shift will be determined by the PD2 voltage (Pin 45), which is generated by the flyback input and the internal Comp1 output. That is related to the H–Drive output transistor storage time.

This function is particularly useful for high frequency scan rates. The higher the frequency, the more significant the storage time becomes, compared to the horizontal scan time.

Figure 5.



7. Proper Horizontal Phase Control

The horizontal adjustment range depends on the phase angle between the H–Sync signal and the horizontal flyback input. In reality, the actual adjustment range is a combination of horizontal frequency, front porch/back porch timing, flyback pulse width, and horizontal output transistor storage time. The following paragraph conveys the concept for normal operation.

There are two clamping situations for video signals. In case 1, separate VTTL and HTTL sync are provided, the video signal is clamped at sync tip, and the dc voltage built up is used for black level reference. In this instance, the clamp pulse has the same pulse width as H–Sync, and nearly the same position. This clamp pulse is blanked out internally. In order to allow the video output to complete the blanking action during horizontal retrace, the horizontal phase should not be over–adjusted. See Figure 6 for a pictorial perception. Accordingly, the total horizontal position adjustment range is calculated as the sum of $\Delta t1$ and $\Delta t2$.

Should the phase of horizontal flyback/H–Sync move further left or right from the normal adjustment range, the black level reference voltage will be restored, and consequently a slightly brighter than screen dark region will be observed on–screen. See Figure 7 for pictorial explanation.

$$\text{Horizontal Blanking Time} = FP_{time} + \text{Sync Width} + BP_{time} = T_{HB}$$

Criterion for Normal Operation:

$$|\Delta t1| < \frac{T_{HB}}{2} \qquad |\Delta t2| < \frac{T_{HB}}{2}$$

In other words, the left/right 0.7 V threshold flyback reference should be within the H–Sync pulse (shaded area of Figure 6).

Figure 6. Horizontal Position Adjustment at Normal Operation

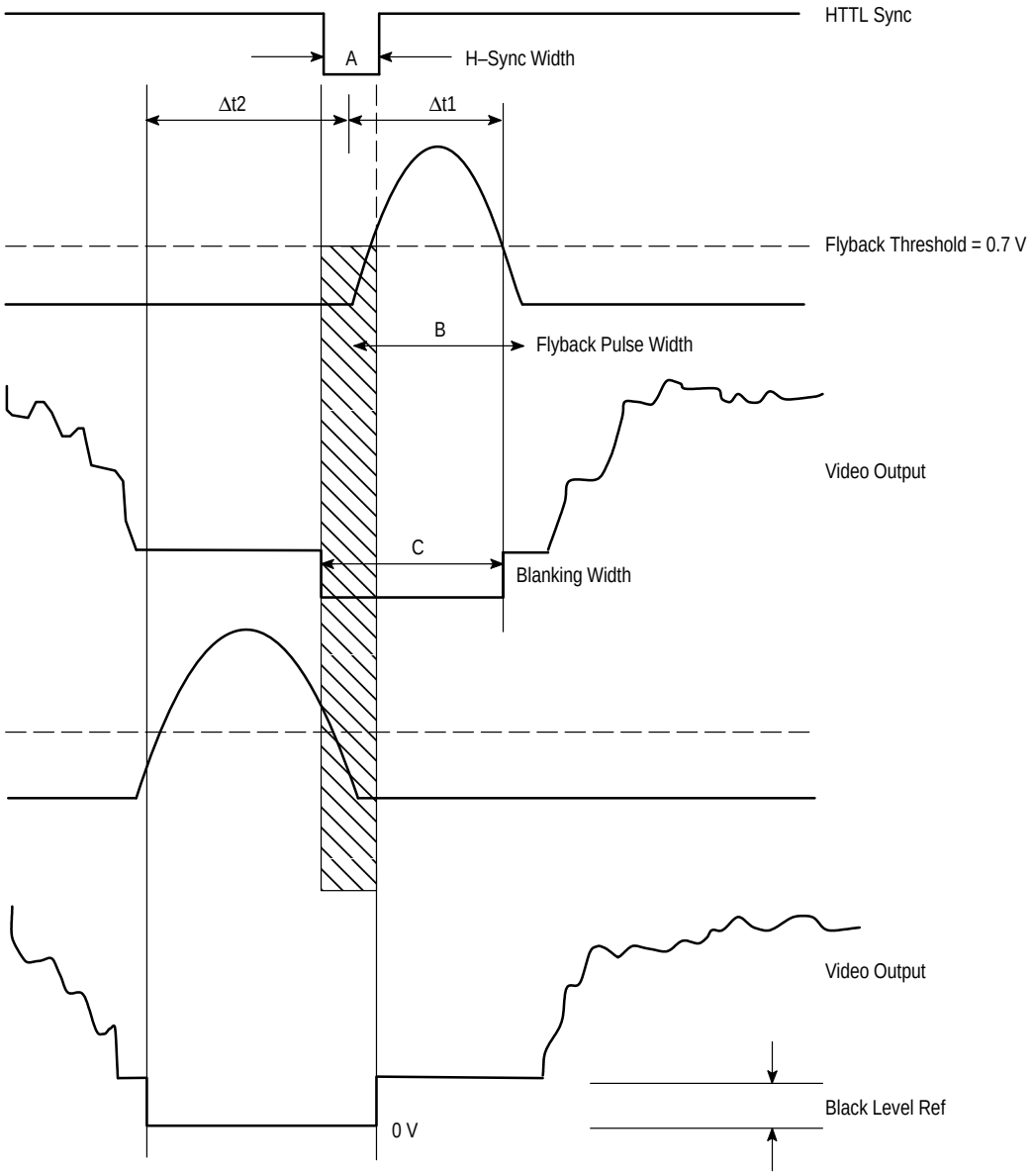
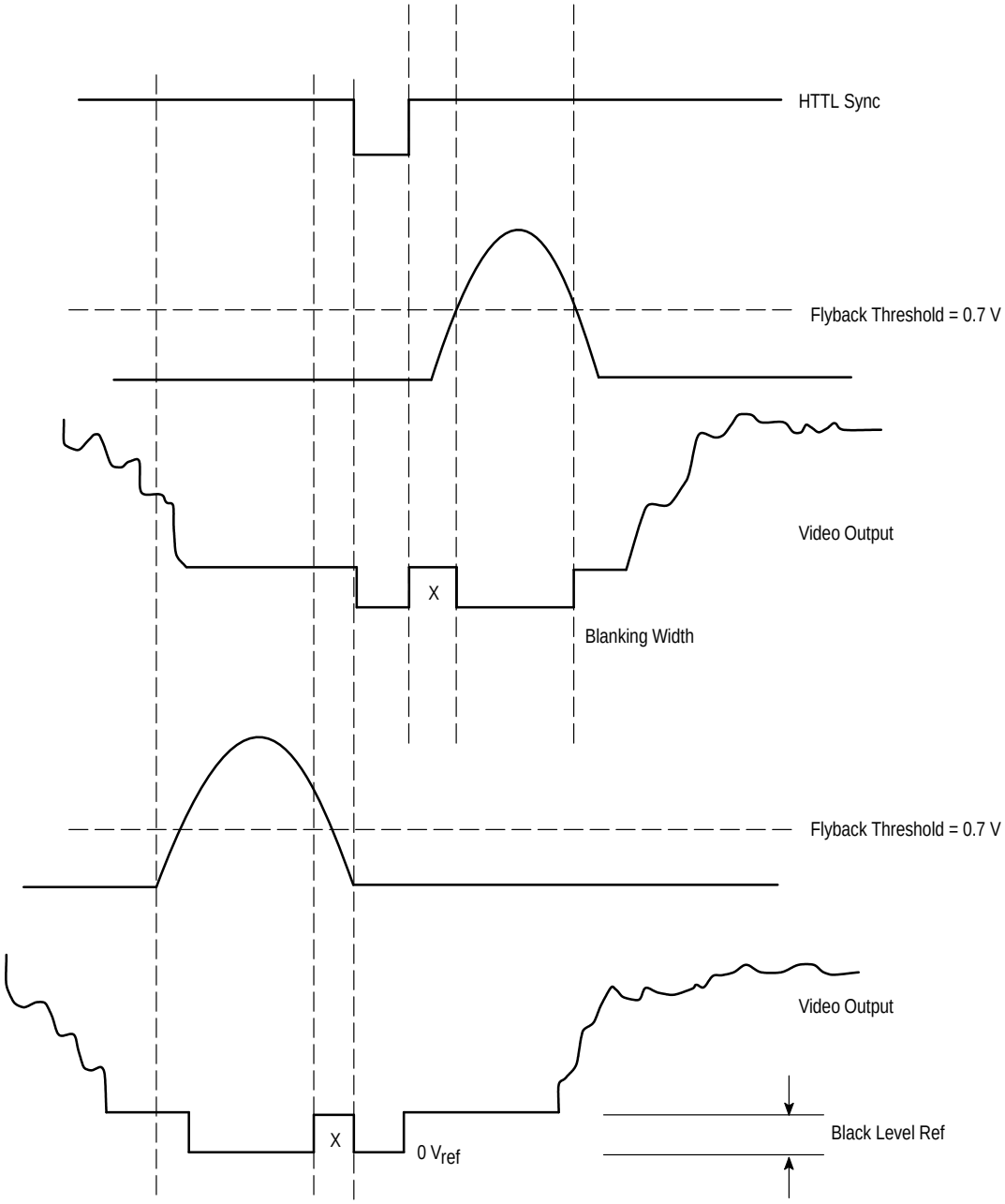
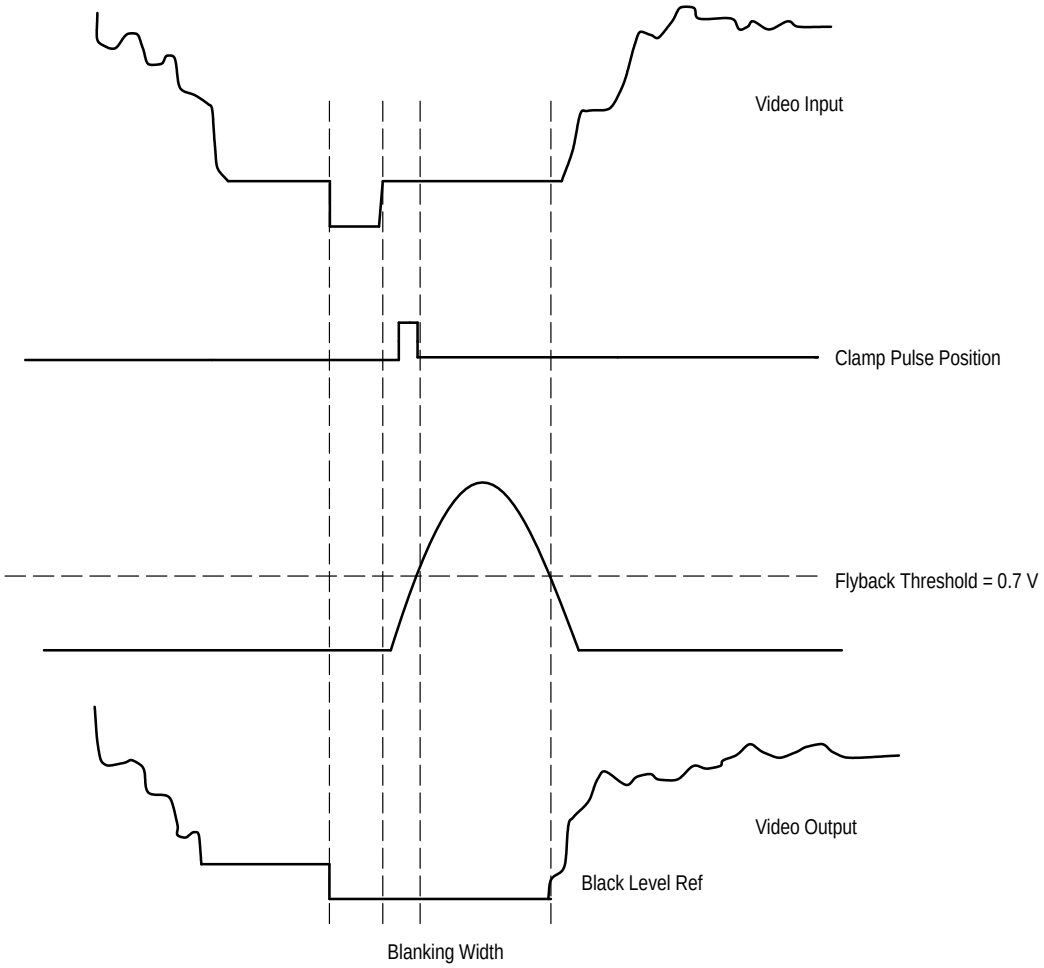


Figure 7. Horizontal Position Adjustment at Overscan Operation



NOTE: Region X will appear as bright vertical stripe.

Figure 8.



In case 2, composite sync is used instead of VTTL and HTTL sync, the clamp pulse is located at the backporch of the video signal, and the width of the clamp pulse is calculated as follows:

$$\text{Clamp Pulse Width} = \frac{1}{64 \times \text{Line Frequency}} \times 3$$

Blanking Width = Sync Width + Clamp Pulse Width + Flyback Threshold (0.7 V) (See Figure 8)

From the above diagram, it can be seen that the horizontal position adjustment is basically the same as case 1 except slightly wider with the addition of clamp pulse blanking.

8. Horizontal Timing Relationship for Phase Detector 2

The following paragraphs explain the PLL2 mechanism. Figure 9 portrays the timing signals of various parts of the IC.

In using the H–Sync pulse, which is generated from PLL1, a horizontal ramp 1 signal is created. H–Ramp1 starts at 1/4th line before H–Sync and the ramping slope is directly proportional to horizontal frequency. The lower tip of this ramp is at approximately 1.2 V, and the amplitude is about 4.2 V. By adjusting the dc bias to the H–Phase control, a pulse waveform is derived from this H–Ramp1.

A phase detector is used to compare the phase between the pulse generated above, and the incoming flyback pulse. An integrating capacitor is applied to generate a dc voltage. This dc voltage, PD2F output, is used to slice the H–Ramp1 signal in order to generate Comp2 output pulse.

A second ramp signal, H–Ramp2, is triggered from this Comp2 output. By applying a dc voltage (H–Width control) to H–Ramp2, the Comp3 output pulses are generated.

The H–Drive output is formed by the rising edge of Comp2 output and the rising edge of Comp3 output.

It can be seen from Figure 9, if the H–Phase control is over or under driven, it will reach the upper/lower tip of H–Ramp1, and thus PLL2 will be disturbed.

Figure 9. Horizontal Timing for PLL2 Internal Sections

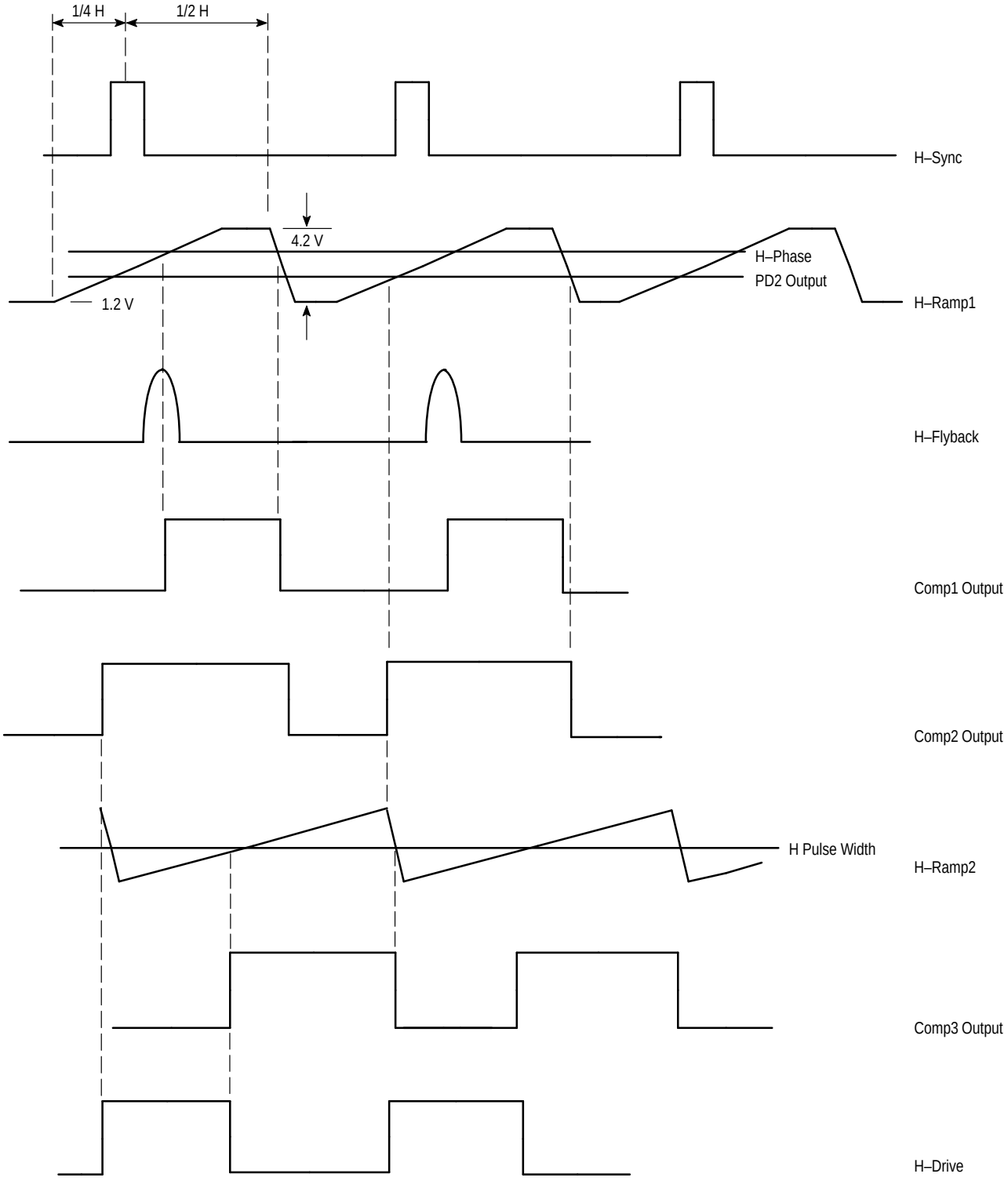
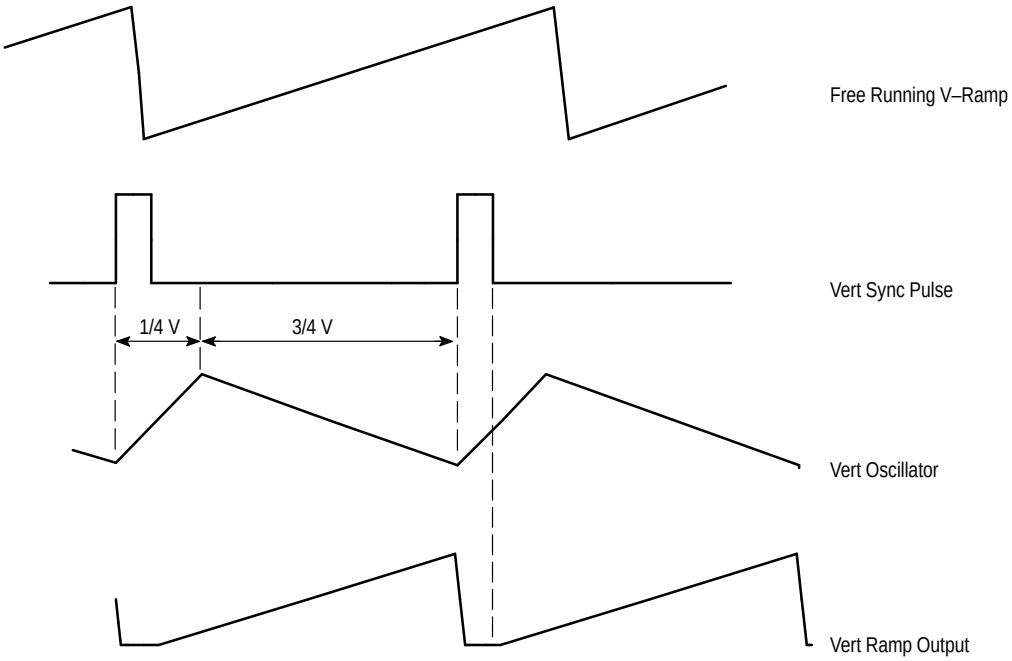


Figure 10. Vertical Section



9. Vertical Frequency Range (Pins 48, 51, 52)

The MC13081X vertical oscillator is an injection–lock type. The device can handle vertical frequency from 45 Hz to 100 Hz.

The internal ramp generator will generate a ramp output in the absence of a V–Sync signal. Upon receiving an external vertical sync pulse, the ramp up portion is forced to retrace, and therefore, the vertical ramp output is synchronized with incoming V–Sync.

The slope of the Vertical Ramp output is directly proportional to the current flowing out of Pin 52. Half of this current is used to charge up the Vertical Ramp Capacitor. As the charging current is increased, so does the ramp slope. External feedback can be provided from Pin 48 to Pins 51 and 52 for linearity adjustment.

10. Vertical Free Running Frequency (Pins 1, 2)

The purpose of the vertical oscillator is to maintain a vertical ramp to the deflection circuitry in the event the vertical sync is not present. Because of the injection–lock type, the free running frequency must be lower than the system's lowest vertical frequency.

While various combinations of C4 and R9 can produce a given frequency, it is recommended C4 be 0.1 μF in order to obtain practical values for R9. The free running frequency should be set at about 10% lower than the minimum operating vertical frequency (54 Hz for a 60 Hz system).

R9 is then calculated from:

$$R9 = \frac{V_{CC} - 1.4}{96 \times C4 \times FV} - 2.5\ k$$

Connecting a potentiometer, (VR2) provides "Vertical Hold" adjustment.

11. X–Ray Shutdown Protection (Pin 41)

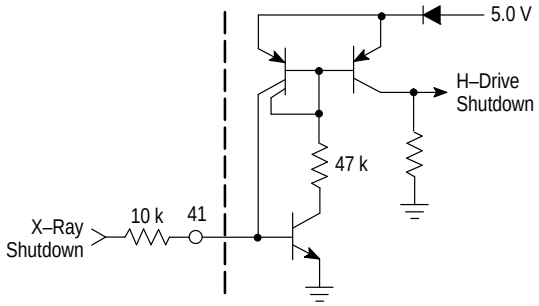
The X–Ray input (Pin 41) permits shutting off the horizontal drive, usually by external circuitry which monitors faults within the high voltage supply, such as excess anode current. This input is activated by taking it above ≈ 0.6 V which causes the drive transistor at Pin 43 to be turned on (low) permanently by an internal latch.

An external resistor must be connected to Pin 41 to limit the input current, and to assist with the latching action (see Figure 11). 10 kΩ is a typical value, but the value can be chosen based on the specifies of the driving circuit. The external resistor reduces the sensitivity of Pin 41 to noise and transients which may otherwise result in false latches.

To resume normal operation (after correction of the fault), lower Pin 41 below 0.4 V. If the external circuit's normal operation does not take it below 0.4 V, but does take it below 0.6 V, then recycle V_{CC} "off"–"on". If the pin is not used, it must be connected to ground.

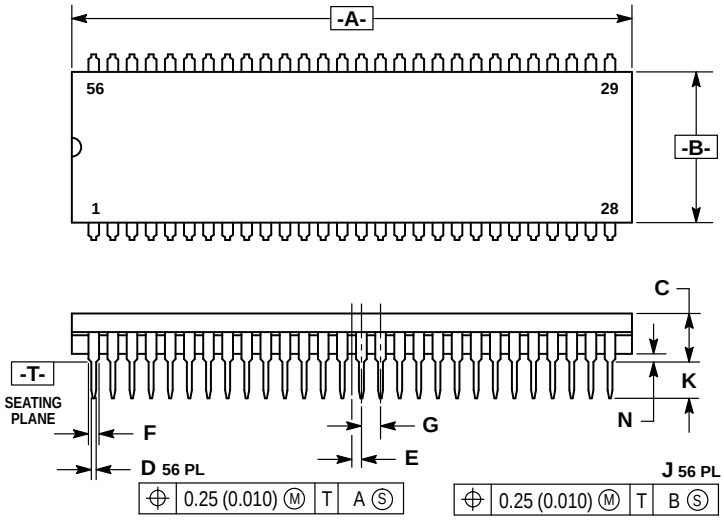
The minimum holding current to keep the latch on is ≈ 70 μA, while the minimum turn–on current is ≈ 0.4 μA.

Figure 11. X–Ray Shutdown Circuit



OUTLINE DIMENSIONS

B SUFFIX
PLASTIC SDIP PACKAGE
CASE 859–01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.035	2.065	51.69	52.45
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
E	0.035 BSC		0.89 BSC	
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

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